CALIFORNIA STATE SCIENCE FAIR
2011 PROJECT SUMMARY

Name(s)

Justin W. Rajewski

Project Number

S0911

Project Title

Utilizing Field Programmable Gate Arrays to Create an Artificial Neural Network Co-Processor

Abstract

Objectives/Goals

As artificial neural networks (ANNs) gain popularity the need for larger and faster networks has arisen. Traditionally when the network is modeled in software the parallel nature is lost as each neuron has to be calculated sequentially. To restore the parallel nature and increase speed, artificial neural networks can be modeled in hardware. The goal of this project is to determine if the speed increase of running ANNs in hardware is enough to merit the use of a co-processor.

Methods/Materials

To test this a FPGA (Field Programmable Gate Array) was used to model the network in hardware and a AVR32 was used to model the network in software. A custom PCB was made where the AVR32 and FPGA were able to communicate over SPI (Serial Peripheral Interface). Both chips ran off the same 33MHz clock for consistency. Once both networks were implemented, each one was timed.

Results

The software implementation utilized by the AVR32 requires approximately 339 clock cycles per neuron in the network while the FPGA requires approximately 12 clock cycles per layer in the network. Due to the parallelism of the FPGA as a network increases in width it requires no extra time to compute, while the software implementation does.

Conclusions/Discussion

For projects that require a large fast ANN, FPGAs provide an effective way to model the network. Large complex real-time ANNs will provide a way to create more advanced artificial intelligence in robots and help in other pattern recognition tasks such as computer vision.

Summary Statement

Using field programmable gate arrays to increase the speed on computing the output of an artificial neural network.

Help Received

FPGA part of the first schematic was reviewed by Luis Maciel, no mistakes were found.