CALIFORNIA STATE SCIENCE FAIR
2015 PROJECT SUMMARY

Name(s)

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Project Number

35495

Project Title

Improved Integrated Circuit Performance by Geometrically Optimized Tri-Gate FinFETs

Abstract

Objectives/Goals

As the technology node gets scaled down aggressively, it is well known that bulk CMOS transistors leak prohibitive amounts of current. Furthermore, capacitive elements in the bulk CMOS substrate channel increase propagation delay. FinFET transistors resolve this with a comparatively lower leakage current. However, to achieve even better leakage and delay values, FinFETs's greater volume compared to bulk CMOS, which increases its parasitic capacitance, is a hindrance.
This work tries to optimize the geometry of FinFET structure and thus tries to lower the leakage even further by lowering capacitance.

Methods/Materials

BSIM's FinFET models were used for experimentation and ideal ranges of values for various FinFET structural parameters were obtained. A separate FinFET model was coded to allow greater flexibility in optimization, and the data from the two was compared. A TCAD modeling tool was also used for non-mathematical electrical simulations.

Results

It was taken care that the performance of the device is not degraded in these experiments. Results obtained are encouraging and can serve as a guideline for realizing new and better derivatives of FinFET.

Conclusions/Discussion

In general, smaller technology nodes displayed the best performance, and substrate capacitance is typically minimal, so the pitch between components must be decreased. With on-state current flowing along the fin's edges and off-state current flowing through the fin's center, decreasing fin thickness should maintain performance while increasing energy efficiency. Finally, increased fin height does not affect parasitic capacitance appreciably but it does increase propagation delay, thus the tradeoff ideal range for fin height lies at around 43-47nm.

Summary Statement

My work aimed to determine the ideal structure and geometry for the Tri-Gate FinFET in order to decrease current leakage, propagation delay, and parasitic capacitance while maintaining on-state current.

Help Received

Participant in Summer Research Program at UC Santa Barbara where I worked under Mr. Shrikant Kulkarni, who was part of Dr. Kaustav Banerjee's Microelectronics Group